[NAME OF THE DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION]

Semiconductor Device and Method for Manufacturing The Same

[SCOPR OF CLAIMS]

[Claim 1] A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a well and an impurity region that is used to electrically connect a lower electrode of the capacitor element and another semiconductor element, wherein the well is located in the semiconductor substrate in the DRAM region, and the impurity region is located in the semiconductor substrate in the analog element region;

(b) simultaneously forming a storage node of the cell capacitor and the lower electrode;

(c) simultaneously forming a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

(d) simultaneously forming a cell plate of the cell capacitor and an upper electrode of the capacitor element.

[Claim 2] A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(e) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (e) is an identical step with the step (d), and

wherein, in the step (e), the number of ion-implantation of impurity in a region where the first resistance element is to be formed is greater

than the number of ion-implantation of impurity in a region where the second resistance element is to be formed to lower a resistance value of the first resistance element than a resistance value of the second resistance element.

[Claim 3] A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(e) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (e) is an identical step with the step (d), and

wherein, in the step (e), an impurity is diffused in a region where the first resistance element is to be formed to lower a resistance value of the first resistance element than a resistance value of the second resistance element.

[Claim 4] A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(e) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (e) is an identical step with the step (d), and

wherein, in the step (e), a silicide layer is formed in a region where the first resistance element is to be formed to lower a resistance value of the first resistance element than a resistance value of the second resistance element.

[Claim 5] A semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the semiconductor device comprising:

an interlayer dielectric layer, impurity region and an embedded connection layer,

wherein the interlayer dielectric layer is located between the semiconductor substrate and the capacitor element,

the embedded connection layer and the impurity region are used to electrically connect a lower electrode of the capacitor element to another semiconductor element,

the impurity region is located in the semiconductor substrate,

the embedded connection layer is located in a connection hole formed in the interlayer dielectric layer,

one end of the embedded connection layer connects to the lower electrode at a bottom surface of the lower electrode, and

another end of the embedded connection layer connects to the impurity region.

[Claim 6] A semiconductor device according to claim 5, further comprising

another capacitor element,

wherein the other capacitor element is located in the analog element region, and

the capacitor element and the other capacitor element are serially connected to each other by the embedded connection layer and the impurity region.

[Claim 7] A semiconductor device according to claim 5 or claim 6, further comprising a first resistance element and a second resistance element,

wherein the first resistance element and the second resistance element are located in the analog element region, and

an impurity concentration of the first resistance element is higher than an impurity concentration of the second resistance element so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.